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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,446	11/28/2003	Yoshinori Shizuno	OHG 146	8271

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EXAMINER	
ROSE, KIESHA L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/722,446	SHIZUNO, YOSHINORI	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-11* is/are rejected.

7)☒ Claim(s) *5 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/03,11/04,1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the filing of the application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,3-4,7 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. (U.S. Patent 6,271,469) in view of Yanagiura (JP 2002-016173)

Ma discloses a die package (Fig. 1j) that contains a semiconductor chip (102) having a first main surface on which a plurality of electrode pads (108) are provided, a second main surface which opposes said first main surface, and a plurality of side surfaces between said first main surface and said second main surface, a liquid resin extension portion (112) which includes a first face and a second face opposing said first face and is formed in contact with side surfaces of semiconductor chip to surround semiconductor chip and such that first face is at a substantially equal level to the level of first main surface, a base (182) (Fig. 6c) having a first surface and second surface which opposes first surface where first surface is contacting second face of extension portion and second main surface of semiconductor chip and has a three dimensional

construction, an insulating film (118) which is formed on first face and first main surface such that a pad of each of plurality of electrode pads is exposed, a plurality of wiring patterns (124) electrically connected to each electrode pads and extended from electrode pads to the upper side of the first surface of extension portion, a sealing portion (126) which is formed on wiring patterns and insulating film such that a part of each of wiring patterns is exposed, a plurality of external terminals (134/138) provided over wiring patterns in a region including the upper side of extension portion and a plurality of conductive electrode posts (132) formed between wiring patterns and external terminals, whereas the external terminals can be solder balls (138) or lands (134) since the extension portion is formed of liquid resin it has a greater molding shrinkage then the molding shrinkage of sealing portion. Ma discloses all the limitations except for the base to be capable of heat generation. Whereas Yanagiura discloses a semiconductor device (Fig. 1) that contains a chip (2), an extension portion (11) that surrounds the chip and a metal base (copper)(11) formed on the bottom of the chip and the extension portion. The base is made of metal to conduct heat and for good heat dissipation. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Ma by incorporating a metal base for good heat dissipation as taught by Yanagiura.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. in view of Yanagiura.

Ma discloses a die package (Fig. 1j) that contains a semiconductor chip (102) having a first main surface on which a plurality of electrode pads (108) are provided, a

second main surface which opposes said first main surface, and a plurality of side surfaces between said first main surface and said second main surface, an extension portion (112) having a concave portion with inclined inside walls, which comprise a first face and a second face opposing said first face and is formed in contact with side surfaces of semiconductor chip to surround semiconductor chip and such that first face is at a substantially equal level to the level of first main surface, a base (182) (Fig. 6c) having a first surface and second surface which opposes first surface where first surface is contacting second face of extension portion and second main surface of semiconductor chip and has a three dimensional construction, an insulating film (118) which is formed on first face and first main surface such that a pad of each of plurality of electrode pads is exposed, a plurality of wiring patterns (124) electrically connected to each electrode pads and extended from electrode pads to the upper side of the first surface of extension portion, a sealing portion (126) which is formed on wiring patterns and insulating film such that a part of each of wiring patterns is exposed and a plurality of external terminals (134/138) provided over wiring patterns in a region including the upper side of extension portion. Whereas Yanagiura discloses a semiconductor device (Fig. 1) that contains a chip (2), an extension portion (11) that surrounds the chip and a metal base (copper)(11) formed on the bottom of the chip and the extension portion. The base is made of metal to conduct heat and for good heat dissipation. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Ma by incorporating a metal base for good heat dissipation as taught by Yanagiura.

Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al.

Ma discloses the claimed invention except for the liquid resin extension portion to have a coefficient of linear expansion and lower temperature range than glass transition temperature and for the base to have a thermal conductivity of at least 150 W/m x K. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the liquid resin extension portion to have a coefficient of linear expansion and lower temperature range than glass transition temperature and have the base to have a thermal conductivity of at least 150 W/m x K, since it has been held that where the general condition of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. (1955)

Allowable Subject Matter

Claims 5 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11

F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1 and 3-8 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1,2 and 4-8 of copending Application No. 10/697247. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the present application are combined limitations of the claims of 10/697247 in regards to the limitation of the base, where the base in the present application is a dependent claim and can just be added into the independent claim. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fukasawa et al. (U.S. Patent 6,455,920) discloses the same semiconductor device as Yanagiura (JP 2002-016173) that disclose a chip, extension portion and base.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KR
KLR

AMIR ZARABIAN
EXAMINER